Determining A Nominal Bit Rate Socket from Spring Probe S-Parameters

Background: When reading the specification on a spring probe, most vendors who market to the high speed functional test market provide an S21 insertion loss plot and usually an S11 return loss plot. This provides information to help evaluate a spring probe for the effects the spring probe will introduce into the test channel when operating through a range of operating frequencies. The S21 plot is usually a good proxy for the pin bandwidth and will provide some information to the engineer if the probe choice is appropriate for the signal rate of the device under test.

Bandwidth and Bit Rate Introduction

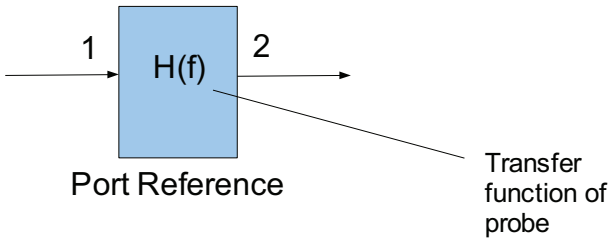
There are a a number of ways to specify bandwidth, all related to the channel application. At its most basic, bandwidth is a measure of the amount of information that can travel through a communications channel. It is usually specified as a frequency for RF modulated analog signals that are sampled and a bit rate for digital binary signals that drive a digital receiver. Bandwidth can be specified in a system as the sum of a number of parallel channels (Bytes/sec). A bandwidth spec is another way to express the Shannon-Nyquist limit for the sampling rate of a communications channel. Often times it is useful to think of a channel as being band limited rather than using bandwidth.

In a test environment for a high speed digital SERDES pin, the basic approximation is that the sampling rate is twice the maximum frequency of the channel. A 1GHz band limited (gigacycles per second) channel supports a bit rate of 2 Gb/s (Gigabits per second) without aliasing- the point where signals in the channel become indistinguishable when sampled. Sampling at higher rates with sophisticated compression and extraction processing hardware allow modern SERDES designs to jam more information and operate at higher rates than the Nyquist limit of a channel specification would imply but that is beyond the scope of this topic.

Signals in a real world passive network like a spring probe and test channel, are always band limited. As the frequency of the signal components increase, more power is lost to the channel. This can be either insertion loss, ie how much of the signal power is seen at the output of the channel, or return loss, how much of the signal power is reflected back to the source. The combination of the insertion loss and return loss of a channel makes up the majority of signal difference observe at the channel source vs. the channel output.

Spring Probe Interface Measurements.

As a passive sub component of a test channel, the spring probe will react across the measured frequency spectrum. As the frequency increases, the probe absorbs the input signal energy. The most common way to express this is with an insertion loss plot from a Network analyzer. This is the S21 plot in a two port network (Output and input) will disply the amount of signal loss across the frequency of the test and express this in -dB.



A loss less component would display a plot at 0dB from the intial frequency to the maximum frequency. A real component will generate a display on the network analyzer that shows the output loosing energy and dropping below a cutoff frequency as the input frequency increases.

Below is a VNA plot of the Insertion loss of the E5533 spring probe. This is an example of a how the probe component will react in a test channel.

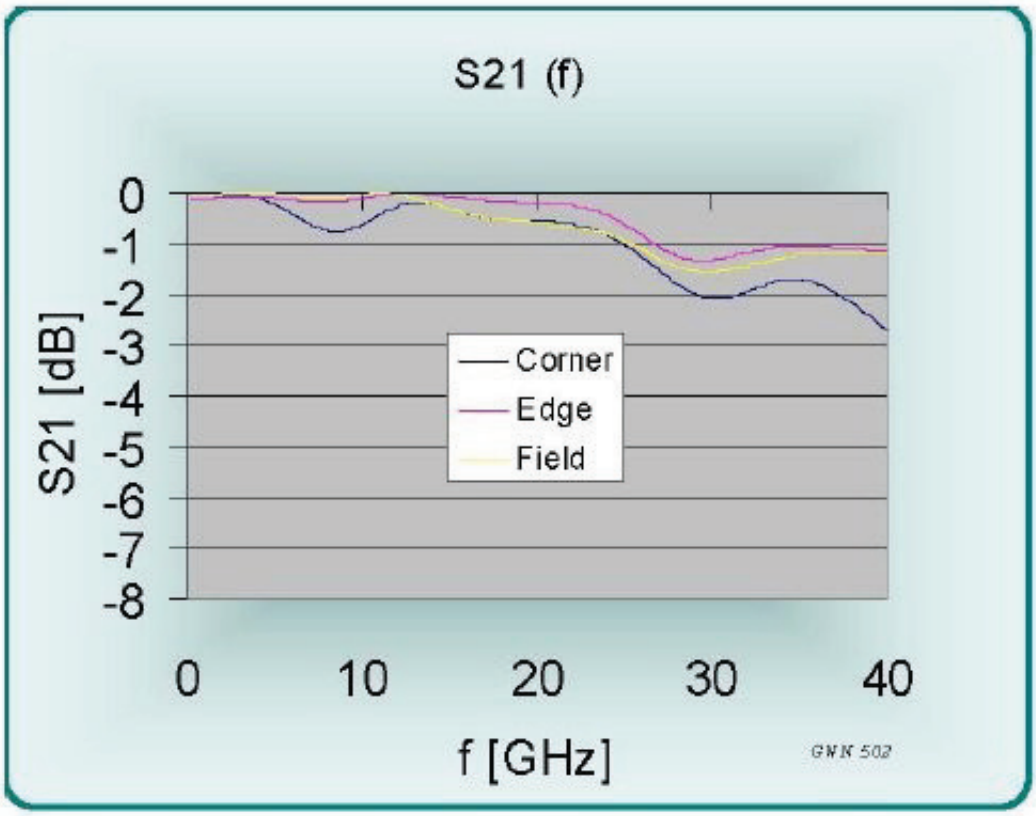


Figure 1: Insertion Loss, S21, E5533-A1

Interpreting this Plot

X coordinate: Frequency, this is 300kHz to 40 GHz a very wide frequency scan.
Y coordinate: Signal Power Loss in dB. This is referenced to the input signal and is a negative measurement. A gain in the signal would register as a positive number.

Bandwidth: The user model for the probe application needs to identify the operating cutoff frequency that is appropriate. Typically, the -1dB cutoff frequency is used to mark the probe pin operating frequency on an S21 plot. In the case of the E5533-A1, this cutoff frequency is 28GHz for the edge pins, and approximately 26 GHz for the Field and corner pin configurations.

Bit Rate: Channel transfer function would equate to a nominal 52-56 GB/s. This is simply the taking the cprobe frequency and doubling the value to achieve the bit rate. This represent an ideal approximation for the bit rate (information rate) that the probe pin is capable of passing.

De-rating the Maximum Bit Rate: A data communications signal consisting of serial binary data is a sum of the full frequency spectrum impulse responses for the bit stream pulses. This effect consists of the harmonic attenuation of the pulses seen at the clock rate of the signal and the attenuation of the edge impulse response harmonics. This attenuation is a result of the natural low pass filter response of the probe pin and other passive components of the test channel. These passive components consist of the integral responses of the distributed transmission line from a board and or cable interface to the probe pin as well as the lumped model structures of the interface board connections such as vias or probe pads. As a rule of thumb, in the presence of no signal conditioning, a channel should be able to pass the signal's third harmonic as well as a large percentage of the 5th harmonic to maintain. How does this effect the maximum bit rate of a probe pin when a serial, digital data stream is key to understanding what frequency a probe pin needs to provide a transparent test.

Serial Data Harmonics

Some examples of bit rates and harmonics:

Protocol	Bit Rate	Harmonics 1st 3rd 5th	Cutoff
FBDIMM2	9.6 GB/s	4.8 GHz, 14.4GHz, 24GHz	24 GHz
PCIe3	8.0 GB/s	4.0GHz, 12.0GHz, 20GHz	20 GHz
FBDIMM3	16.0GB/s	8.0GHz,24 GHz, 40 GHz	40 GHz
Coherency Protocol	20 Gb/s	10 GHz, 30 GHz, 50 GHz	50 GHz

This table gives us a projected frequency needed for the probe pin to provide minimal attenuation to the signals 5th harmonics and is transparent in the time and voltage domains. probe pins that have enough bandwidth to pass the target signal's 5th harmonics will exhibit very low channel ISI and DCD. This frees the engineer to concentrate on less forgiving components in the signal interface. The fact is that a serial data signal has high frequency components above the clocked bit rate that the probe pin and test channel need to support

Eye Opening

Another way to estimate the bit rate of a channel is to estimate the point where the eye is closed 35%. Eye closure in a serial bit stream is a result of the voltage loss in the channel, the loss of signal rise time due to the capacitance and channel time constant and the eye closure from Intersymbol Interference (ISI) due to group delay in the channel elements. A perfect 1V 100 ps wide eye would still be useable based on a a protocol eye template. An engineer looking at an S21 plot with a -1dB cutoff could extrapolate to the 3 dB cutoff to estimate the 65% eye opening loss from the probe pin.

Since a probe has to operate in a complete test channel, the probe contribution to the total loss is small. The probe is a small percentage of the total channel length and as a lumped element there is a sum of the squares function of all the lumped elements in the total channel loss. As an estimate, the -2dB cutoff point for the probe can be used to estimate the 3% eye closure contribution of the probe pin.

Linear estimate to extrapolate the -2dB eye opening for the -1dB S21 loss is impossible from the S21 plot alone. Adding up all the components we can be confident that the probe will exhibit a 15-20% bit rate increase over the clocked bit rate at -2dB operation rather than -1dB operation.

Serial Data Compensation

Modern Serdes transceiver pairs have implemented many architectural features to process the data in a lossy channel. A transmitter/receiver pair in a Serdes lane can usually be designed to operate in loss environments that approach and exceed -20dB. Using real time DSP, de-emphasis, Finite Impulse Response circuitry, advanced CDRs, and pulse shaping, a Serdes lane can often train and operate when the eye observed in the test channel is completely closed. What does this mean for the probe pin response?

The probe/interface should provide a smooth loss curve to insure that -2.2 the probe adds minimal lumped distortion points. Large frequency notches on an S21 curve may cause too much variability in pattern discernment functions and inhibit the lane performance. A lossy probe pin at high frequency may be perfectly adequate to test a device IO as long as the loss remains fairly linear. A resonance spot can be highly detrimental and probe - board via interfaces can produce these resonance points as a function of the probe-via Tpd. Resonance is closely related to a quarter wavelength cancellation.

For instance at 10 GHz, a resonance point would occur in a via-probe discontinuity of 295 mils. At 50 GHz, this resonance is at 59 mils or 1.5mm. These points can cause problems in the DSP selecting a 1/0 in the bit stream by ultra-attenuating the harmonic frequencies present in a high speed serial bit stream. This puts a hard limit on the upper bit rate performance for a particular via-probe stack.

Signal Integrity Spring Probes - Projected Bit Rates

0.4mm Pins

Probe	-1dB Cutoff	Clocked Bit Rate	Full Harmonic Bit Rate
AA909	12.0 GHz	24 Gb/s	4.8GB/s
A1512	20.3 GHz	40.6 Gb/s	8.12Gb/s
A1520	24.1 GHz	48.2 Gb/s	9.64Gb/s
A1540	16.1 GHz	32.2 Gb/s	6.44Gb/s
A1550	18.7 GHz	37.4 Gb/s	7.48 Gb/s
A1561	7.4 GHz	15.4 Gb/s	3.08 Gb/s
A1562	11.6 GHz	23.2 Gb/s	4.64 Gb/s
A1580	7.4 GHz	15.4 Gb/s	3.08 Gb/s
A1582	9.6 GHz	19.2 Gb/s	3.84 Gb/s

Clocked Bit Rate = 80% Eye opening, loss less channel estimate. Full harmonic Bit Rate is the inside marginal spec for the probe where no observable distortion is present

0.5mm Pins

Probe	-1dB Cutoff	Clocked Bit Rate	Full Harmonic Bit Rate
B2500	6.4 GHz	12.8 Gb/s	2.94 Gb/s
B2501	11.2 GHz	22.8 Gb/s	4.56 Gb/s
B2502	17.0 GHz	34 Gb/s	6.8 Gb/s
B2503	13.0 GHz	26 Gb/s	5.2 Gb/s
B2504	8.8 GHz	17.6 Gb/s	3.52 Gb/s
B2509	16.1 GHz	32.2 Gb/s	6.44 Gb/s
B2514	12.2 GHz	24.4 Gb/s	4.88 Gb/s

Clocked Bit Rate = 80% Eye opening, loss less channel estimate. Full harmonic Bit Rate is the inside marginal spec for the probe where no observable distortion is present

0.8mm Pins

Probe	-1dB Cutoff Frequency	Clocked Bit Rate	Full Harmonic Bit Rate
D4525	19.5	39 Gb/s	7.8 Gb/s
D4565	17.0 GHz	34 Gb/s	6.8 Gb/s
D4595	19.5 GHz	39 Gb/s	7.8 Gb/s
D4601	12.8 GHz	25.6 Gb/s	5.12 Gb/s
D4603	12.4 GHz	24.8 Gb/s	4.96 G/s
D4613	14.3 GHz	28.6 Gb/s	5.72 Gb/s
D4623	8.2 GHz	16.4 Gb/s	3.28 Gb/s
D4693	18.3 GHz	36.6 Gb/s	7.32 Gb/s

Clocked Bit Rate = 80% Eye opening, loss less channel estimate. Full harmonic Bit Rate is the inside marginal spec for the probe where no observable distortion is present

1.0 mm pitch pins

E5566	>40 GHz	80 Gb/s	16 Gb/s
E5533	25.3 GHz	50.6 Gb/s	10.12 Gb/s
E5548	14.5 GHz	29 GB/s	5.8 Gb/s
E5585	31.5 GHz	63 Gb/s	12.6 Gb/s
E5593	31.5 GHz	63 Gb/s	12.6 Gb/s
E5656	13.9 GHz	27.8 Gb/s	5.52 Gb/s

Clocked Bit Rate = 80% Eye opening, loss less channel estimate. Full harmonic Bit Rate is the inside marginal spec for the probe where no observable distortion is present.