
SII Coaxial Spring Probe Solution Comparison of Performance of Coaxial vs Non- Coaxial Spring Probes Used

Background

A socket/board designer faces a number of conflicting requirements in selecting a spring probe for a socket. The spring probe needs to fit the package pitch, handle the maximum per pin current, and perform as a high frequency interface. In addition the board to spring probe interface creates discontinuities that create insertion loss non-linearity. Finally large SOC devices can exhibit extremes of non-planarity that the spring probe travel compliance must handle with an acceptable contact resistance. This compliance issue will often preclude using shorter spring probes with adequate frequency cutoff to achieve the device rated operating speeds.

Example Device Test Requirements

In this white paper we address the problem of testing a SERDES IO that uses a number of signal processing techniques to achieve 16 Gb/s operation. The part self-tests using DFT circuitry so the interface problem consists of a socket and trace/via board interconnecting a Receiver/Transmitter pin pair on the DUT. The primary choices made in board layout are achieving a specific insertion and return loss at the target bit rate and insuring that the insertion loss is linear through the bit rate frequencies.

This paper uses simulated board and spring probe performances using Simbeor THz 3D Modeling and linear network solvers to test the possible socket solutions that are available on the SII website - Signal Integrity Data Sheets.

Channel Model:

The channel model consists of the following components:

- 1) Rx VIA- tuned for 1mm pitch, layer board
- 2) 22.5 inch symmetrical strip line trace
- 3) Nelco 4000-20 core and prepreg, RTF copper - Roughness Factor of 2; 7 uinches RMS.
- 4) 30° trace etch- trapezoidal.
- 5) Target 42.5 ohm impedance.

The model parameters are set for lossy metal and dK and Df parameters for material are based on multi-pole parameters from the manufacturer. A 4 pole Debye dielectric model is used. Bottom line is we are attempting to minimize approximations to real world PCB manufacturing.

Via Model:

In figure 1, we see the cross section and top view of the array via and an adjacent GND pin typical of the launch within the DUT grid. We use layer 4 since it is in the mid point of the signal layer laminates.

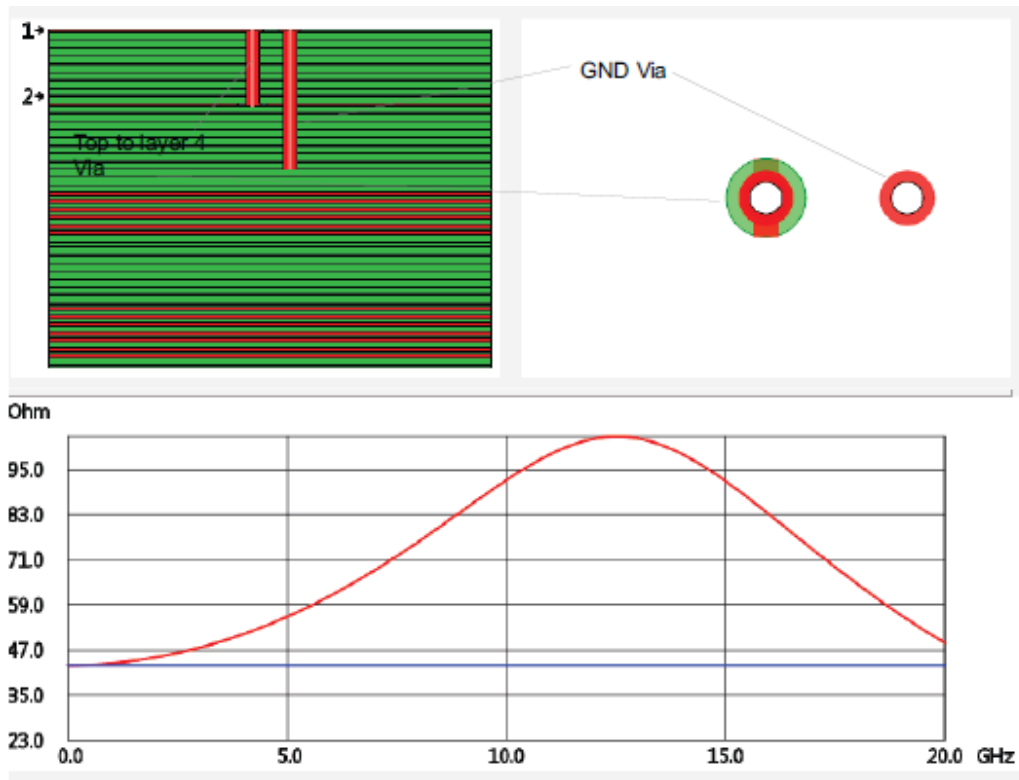
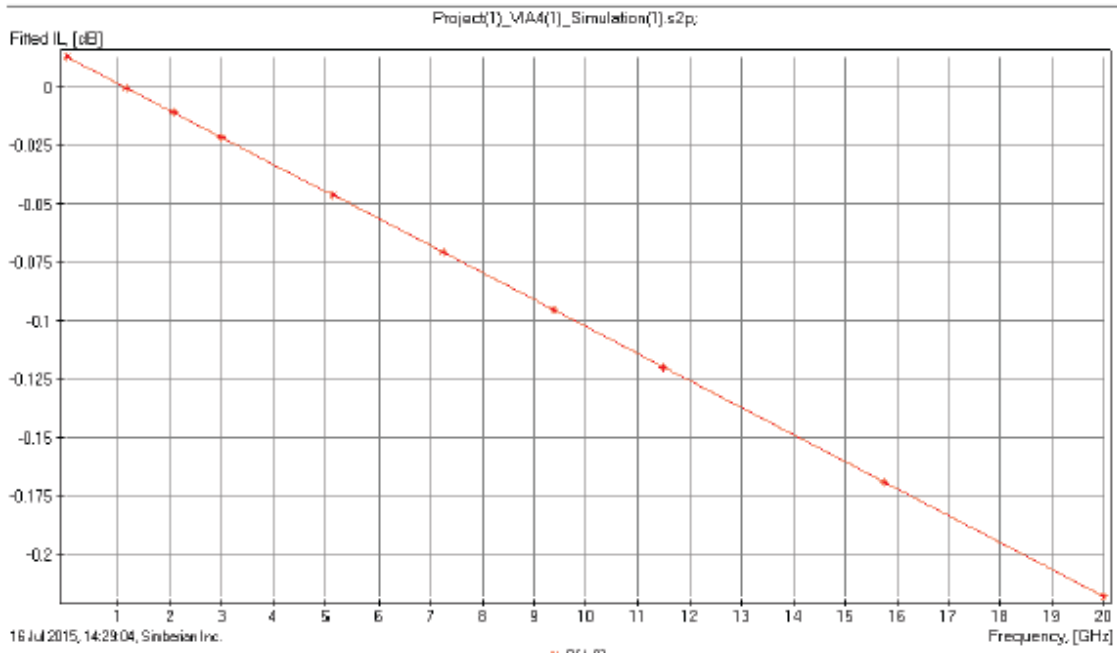


Figure 1

The impedance vs frequency graph of the via is also shown. Over frequency the impedance of this via varies a great deal and is a challenge to match pin probe performance.

However, the short path length of the via shows minimal insertion loss to 20 GHz.



The return loss for the via is also well defined at -20dB at 10 GHz.

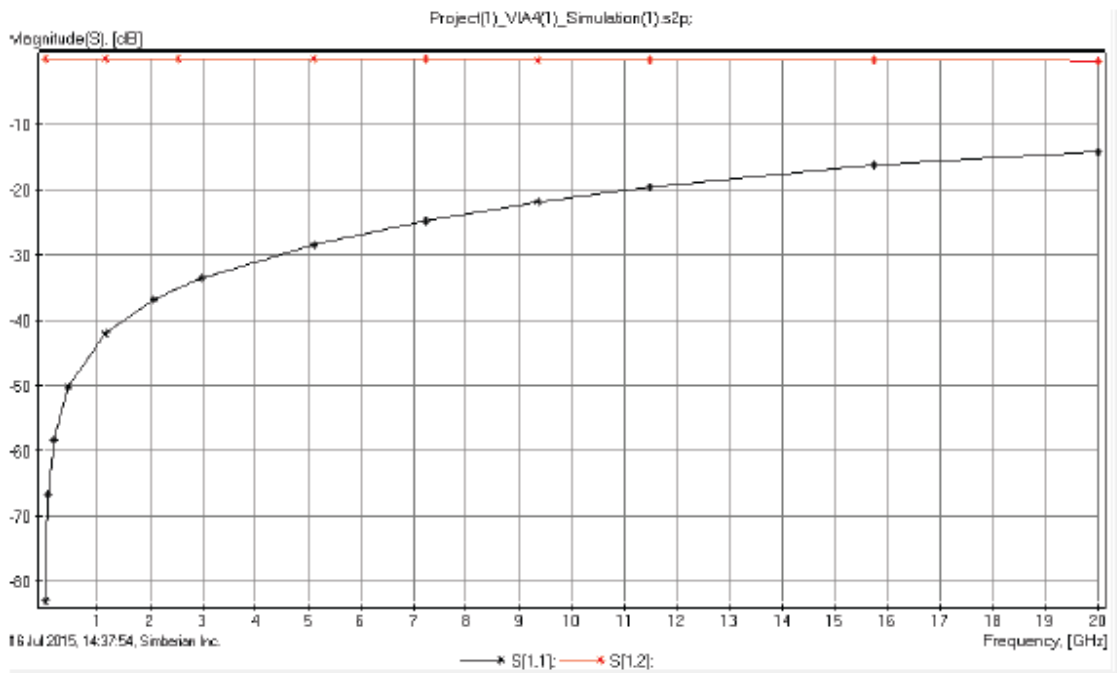


Figure 2 insertion and return Loss for layer 4 VIA

Note, This assumes a one layer back drill accuracy (14 mils) larger back drill tolerances effect this performance a great deal.

Adding a 22.5 inch trace to the vias we find that the insertion loss for the board is calculated with the trace model in figure 3. This is a 200 mil segment of the trace which is then extended to 22.5 inches in a linear network solver.

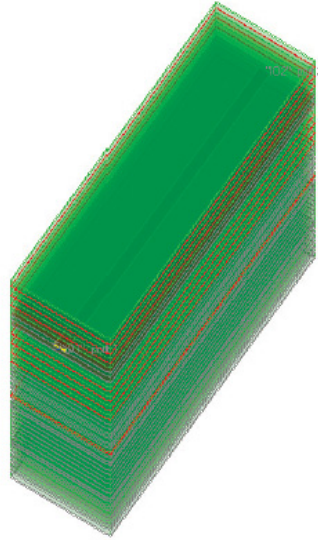


Figure 3 - 3D Trace model for Layer 4

Simulating the trace we find that the loss per mm is -0.029 dB at 10 GHz and the impedance holds under 43 ohms to 20 GHz. The impedance result is expected since this is modeled as a straight trace so there are no bends to change the wavelength (Figure 5)

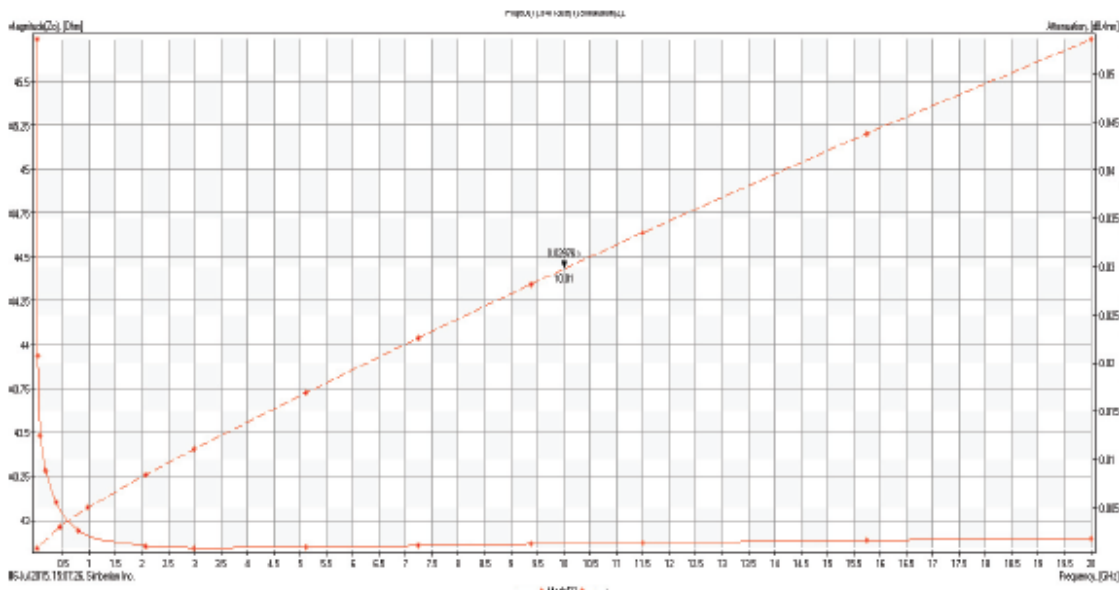


Figure 5 Trace Segment 3D Simulation

Establishing Correlation Baseline Model

Now we create a linear network using the Via model and trace model to establish a base line and correlate to a test trace on an actual board. This correlation step is important to establish the modeling accuracy to real world results and establish the effects of the pogo pin/socket in the model will relatively correlate to real world signal degradation. (Figure 6)

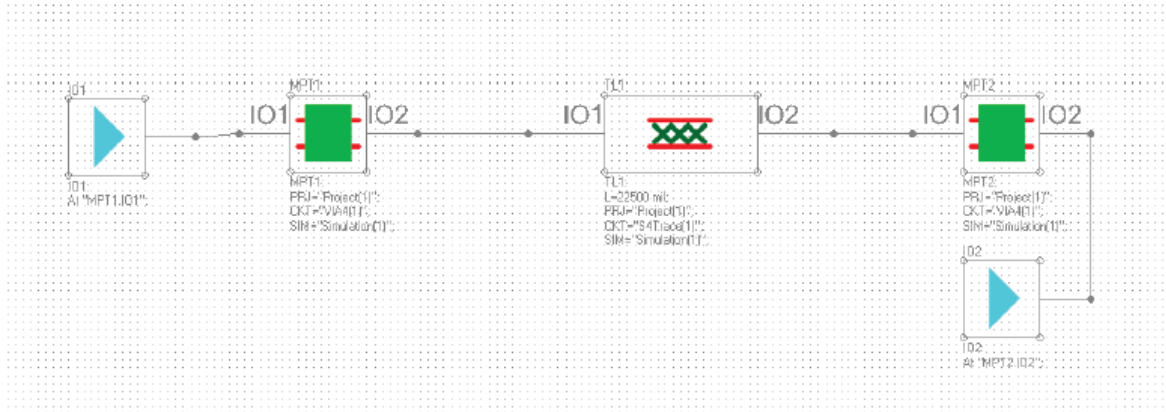


Figure 6
Network Simulation Schematic for Board Trace

Now we calculate the S21 and S11 parameters for the board via trace model as shown in figure 7. S21/12 at 10 GHz is -17.13 dB and S11 at 10 GHz is -19dB at 10 GHz

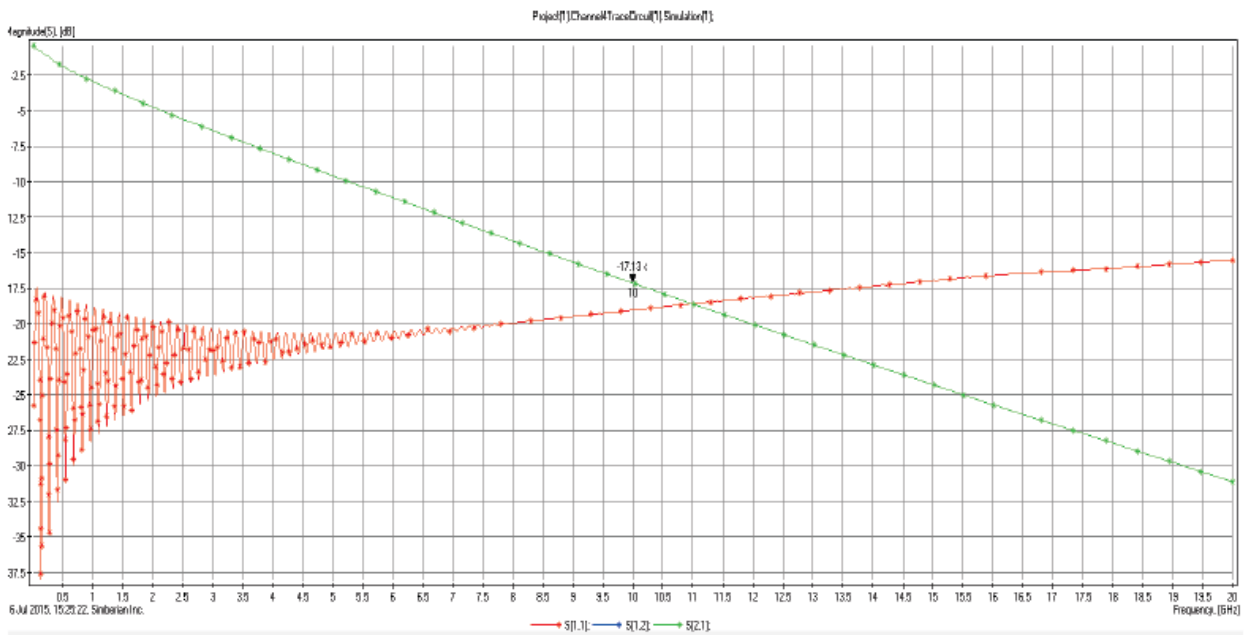


Figure 7
S21 and S11 for Baseline Board Test Channel

This correlates well to the actual VNA measurements for a test trace built with the same design dimensions using NELCO 4800-20 material. The VNA graph is shown in figure 8.

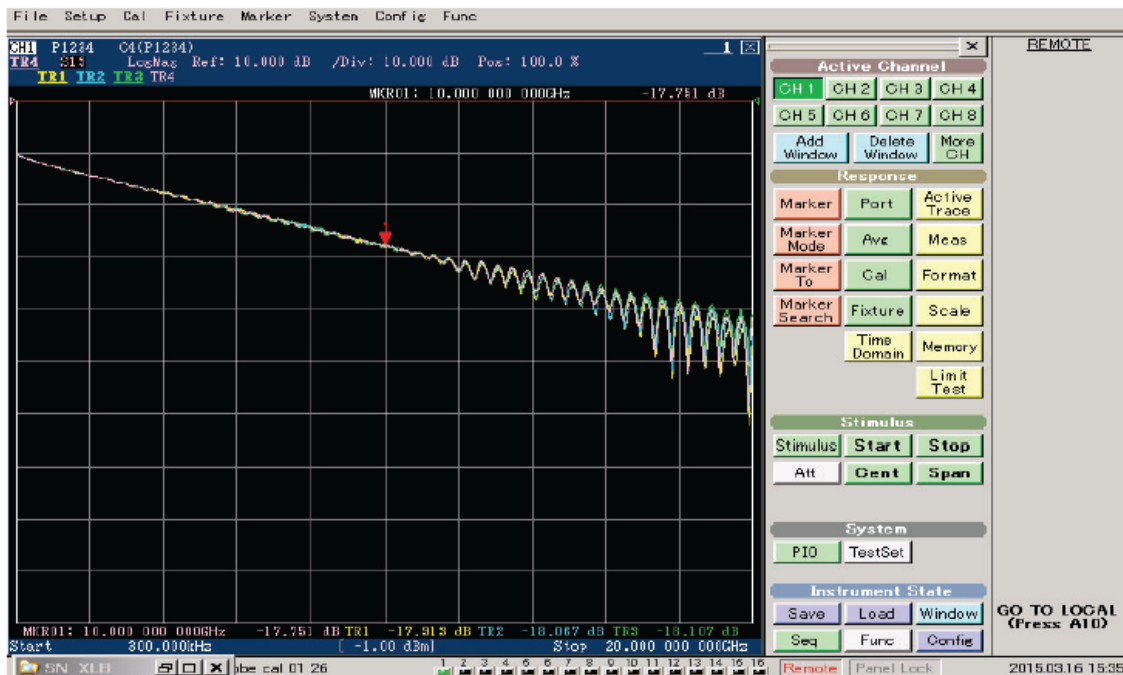


Figure 8 VNA Measurements of Model to Board Trace Test Structure

The VNA plot shows very good physical correlation. Loss at 10 GHz is -17.75 dB on the VNA. The additional loss can be accounted for in the non-ideal probing system (40 GHz pico probes), non-ideal probe inductance and capacitance, and trace and impedance variance from nominal with manufacturing tolerances and imperfections. It is sufficient to establish the baseline model as a good starting point to model and measure the effects of the probe selection on channel performance.

The higher frequency oscillations can be linked to the plane and dielectric resonances that are not accounted for in the simulator or filtered out by the solver. As well, trace impedance shifts due to layout bends versus the straight trace mode and low frequency artifacts that are below the minimum simulator cutoff are also eliminated in the simulation.

Choosing a Probe and Modeling the Channel

SII provides an extensive set of characterization data and both lumped SPICE models and Touchstone/transmission line models for the spring probes in their catalog. We will look at the effects of three probes on the simulated results of the and the historical path to choosing to go with a coaxial model socket from SII.

The first probe selected to test this large package, highly scaled, high powered, high speed IO part was the E5533 (E5533 Specifications). This part was chosen for its high per pin current capacity of 8 amps, and high -1dB cutoff of 25 GHz to provide margin over the target IO frequency.

In the channel model we used the published lumped PI model provided by SII shown in figure 9. Our target is 10 GHz so the model is valid and meets causality and passivity requirements for the linear network.

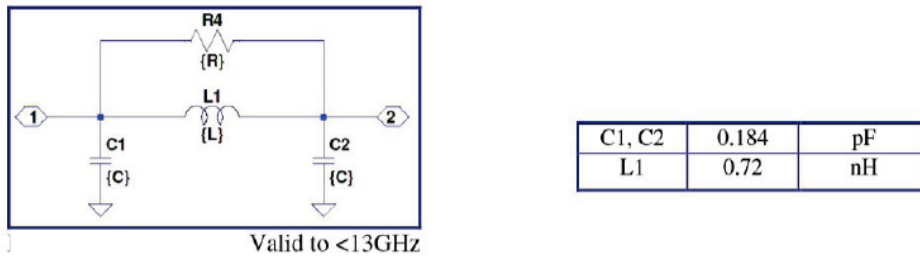


Figure 9 E5533 Lumped Model

Figure 10 is the simulated S21 and S11 parameters for the E5533 lumped model. The 10 GHz cutoff is -0.32 dB and the return loss is well controlled under -15dB to 13 GHz.

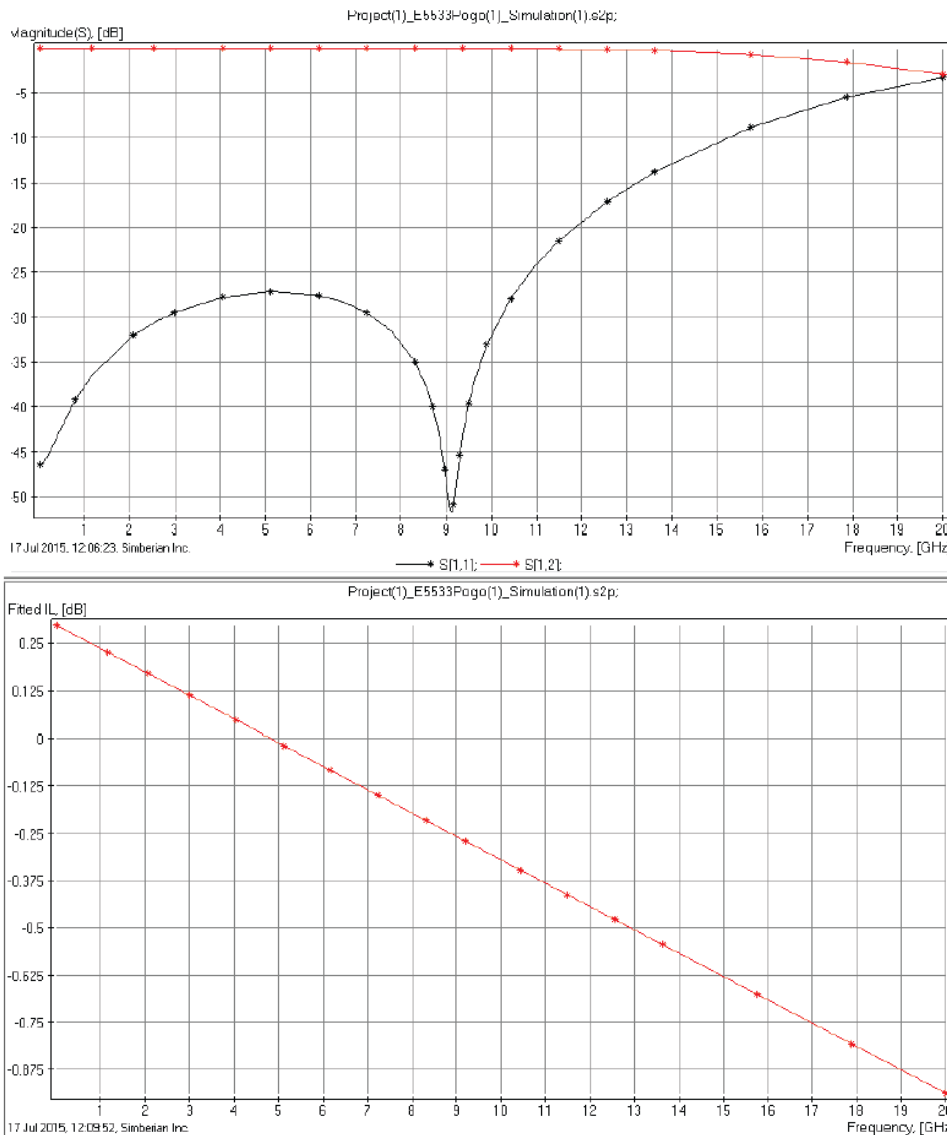


Figure 10 - S Parameters and Fitted Insertion Loss for E5533 Lumped Model

Now adding the E5533 model to the channel model and comparing the S21 plots for each yields

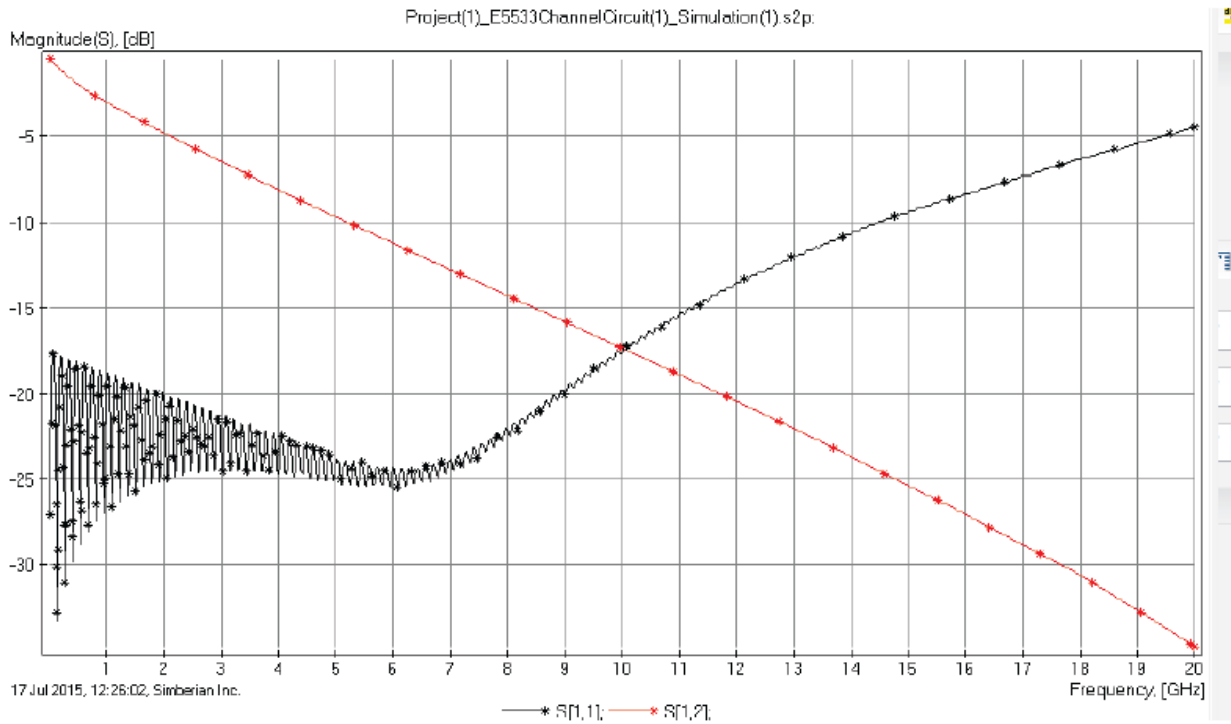


Figure 11

The E5533 degrades the baseline channel -0.58dB at 10 GHz. The return loss degrades slightly over the socket-less channel but is still acceptable. Comparing the fitted insertion loss and Insertion loss deviation shows excellent correlation to 14 GHz.

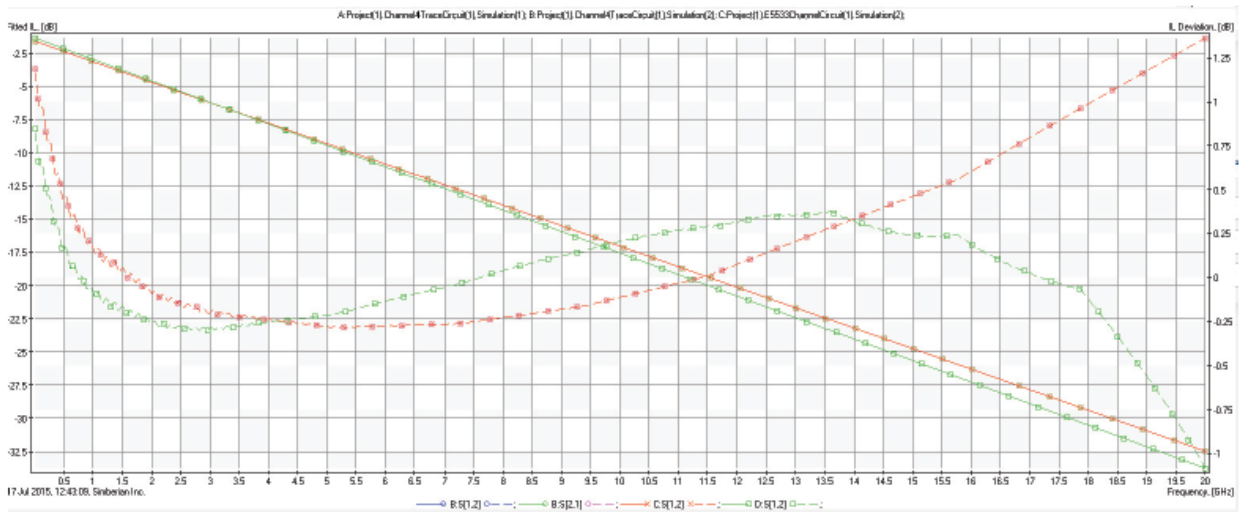


Figure 12
Insertion Loss comparison

So for this application the E5533 is quite good to 14 GHz on the lumped model and would be a good choice for the socket.

Package Considerations

Unfortunately one aspect of the device did not allow us to reliably interface with the E5533 populated socket. This was due to a constraint introduced by the very large package and the variance in the package planarity on the pin side of the grid. This required a great deal more travel than the E5533 could provide. As a compromise the D4697 (D4697 Specification) was chosen and the contact reliability problem solved. However AC performance is degraded somewhat.

We use a simulation of the field lumped model since the majority of the SERDES pins operate inside the array boundary. Since the lumped model is good to about 6 GHz, the lumped model and a transmission line model need to be integrated to project the correct loss at 10 GHz.

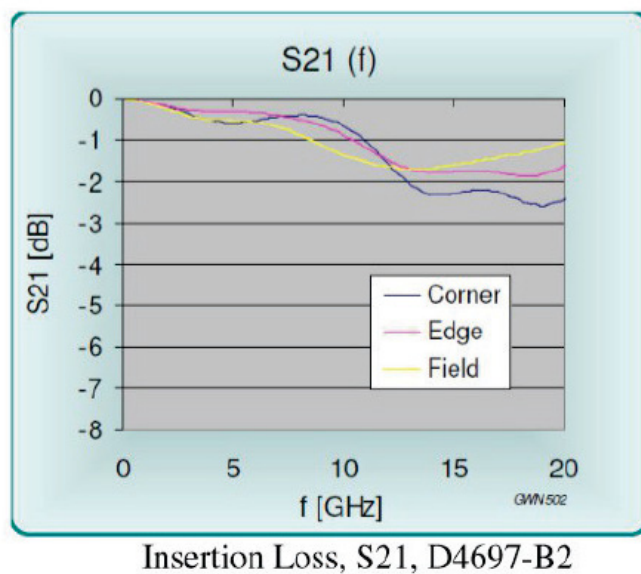


Figure 13 VNA Measured Insertion Loss for D4697

The Lumped Model Field Insertion loss is shown below in Figure 14. The -1dB cutoff is approximately 6 GHz. However this doesn't correlate too well with the VNA measurement and as stated in the SII spec sheet, the distributed model needs to be integrated to find the high frequency operating points.

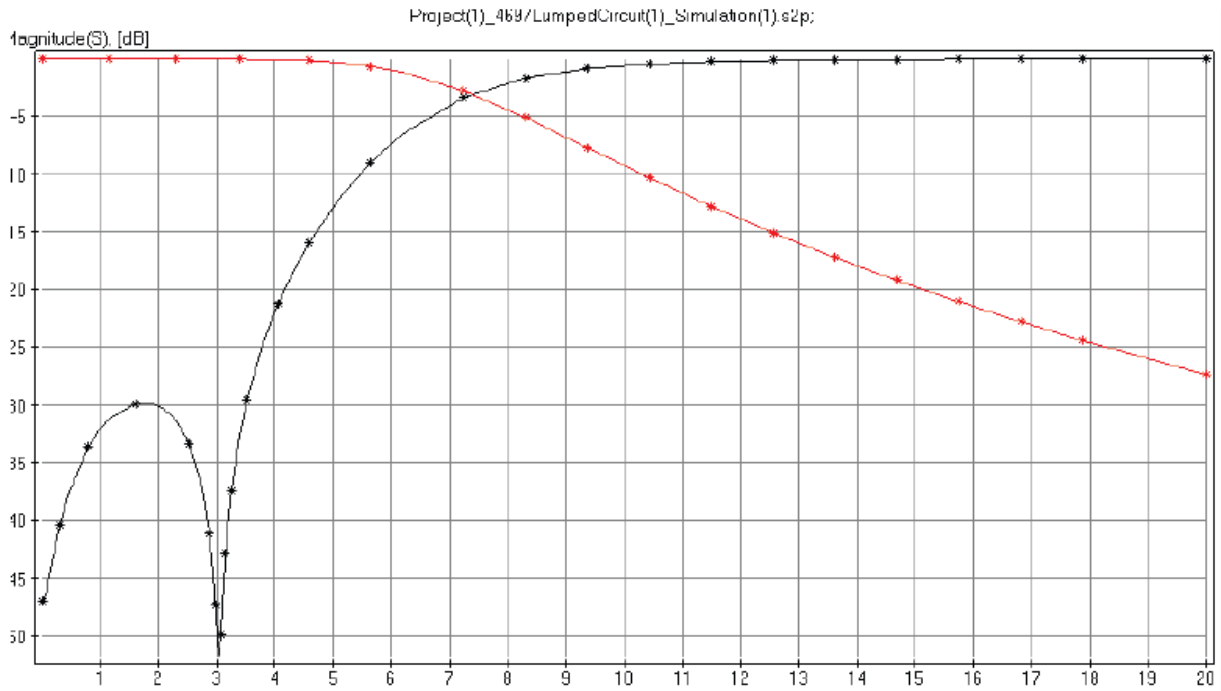


Figure 14 Lumped model from specification

Using a linear regression and a bit of curve fitting on the model parameters to intersect the transmission line model for the D4697 yields a better fit with the VNA measurements.

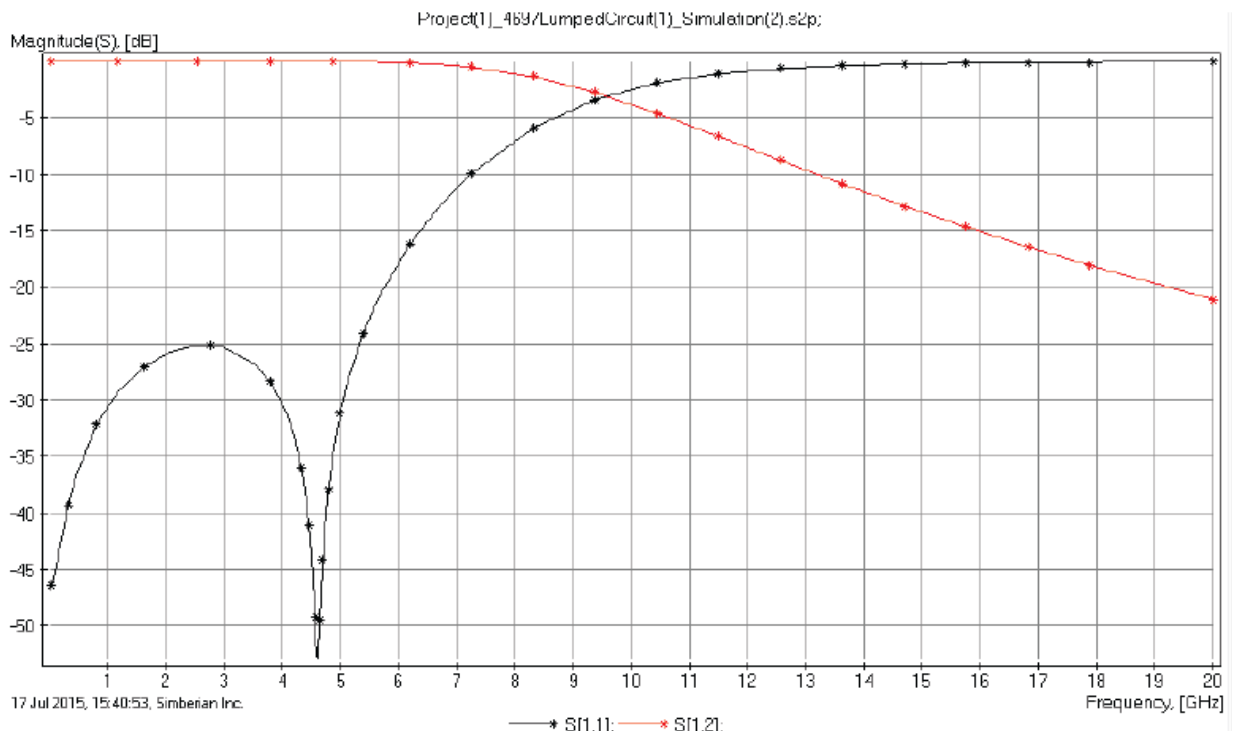


Figure 15

Lump/Transmission Line Model Normalizing Performance to Correlate to VNA measurements

Solving for the full channel solution gives us:

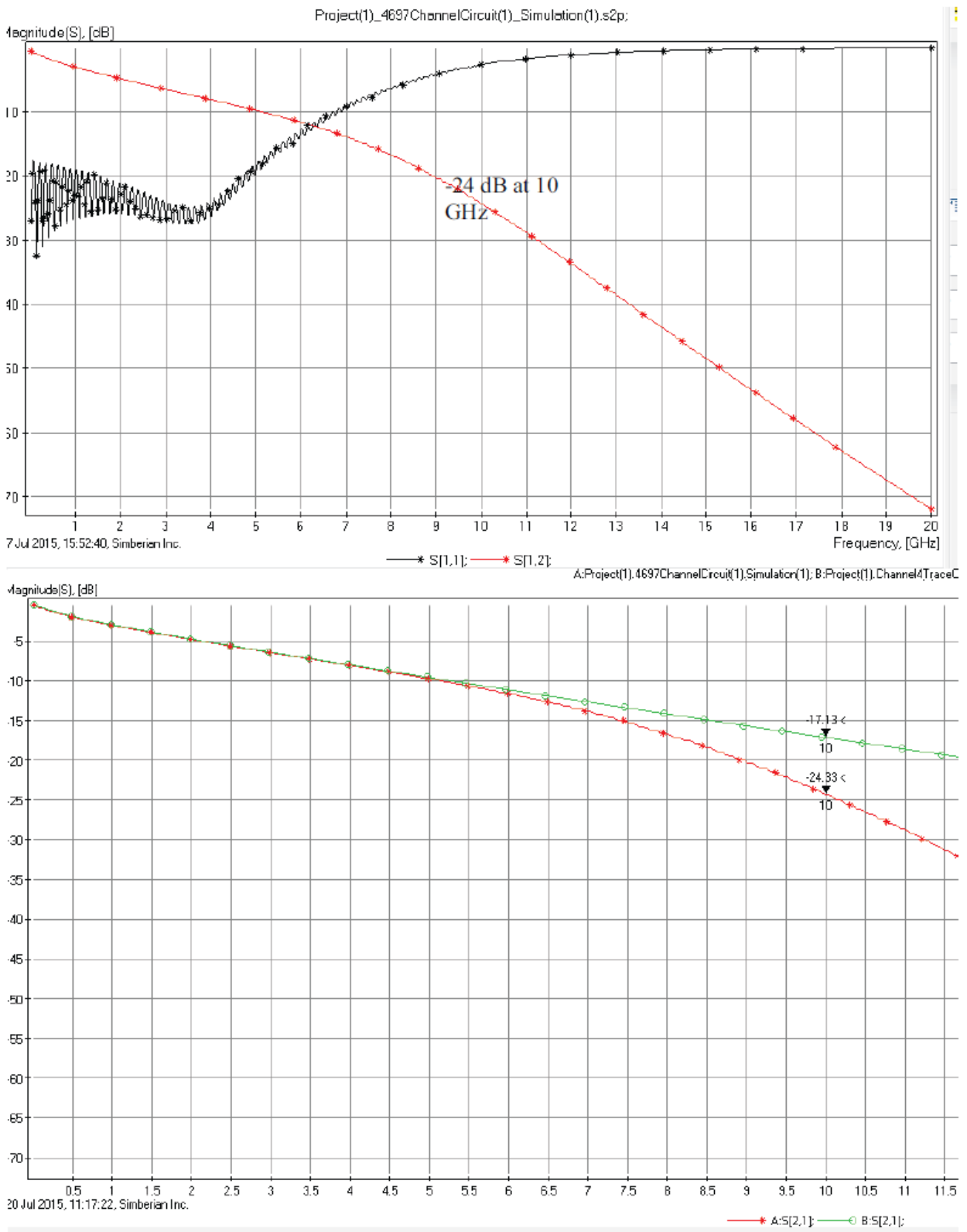


Figure 16 Comparing 4697 Performance to Baseline

The green trace is the base channel, and the red trace is the same channel with a 4697 probe. The insertion loss degrades -6dB at 10 GHz using the D4697 pins. Since the compliance is a fixed requirement, i.e. connectivity comes before anything else with a socket, the end user is forced to adjust test conditions and fit the process to the socket to account for this performance hit and continue to yield. Also, pushing this design 10 test rate faster will be problematic above 14 GB/s as the curve fit exceeds the device ability to channel adjust in its DSP.

Ideally what is needed is the compliance of the 4697 mechanical design and the AC performance of a pin like the E5533.

Coaxial Socket Solution

The end user settled on a full coaxial solution to achieve the goals of higher bandwidth AC 10 performance and high compliance. Using an long high compliance SII spring probe and socket technology for building a coaxial probe channel, a design was chosen that matched the board impedance as closely as possible and pushed the insertion loss back to linear to 20 GHz.

Modeling the coaxial socket pin

A 3D coaxial model was used and S-parameters extracted. Results are in Figure 17.

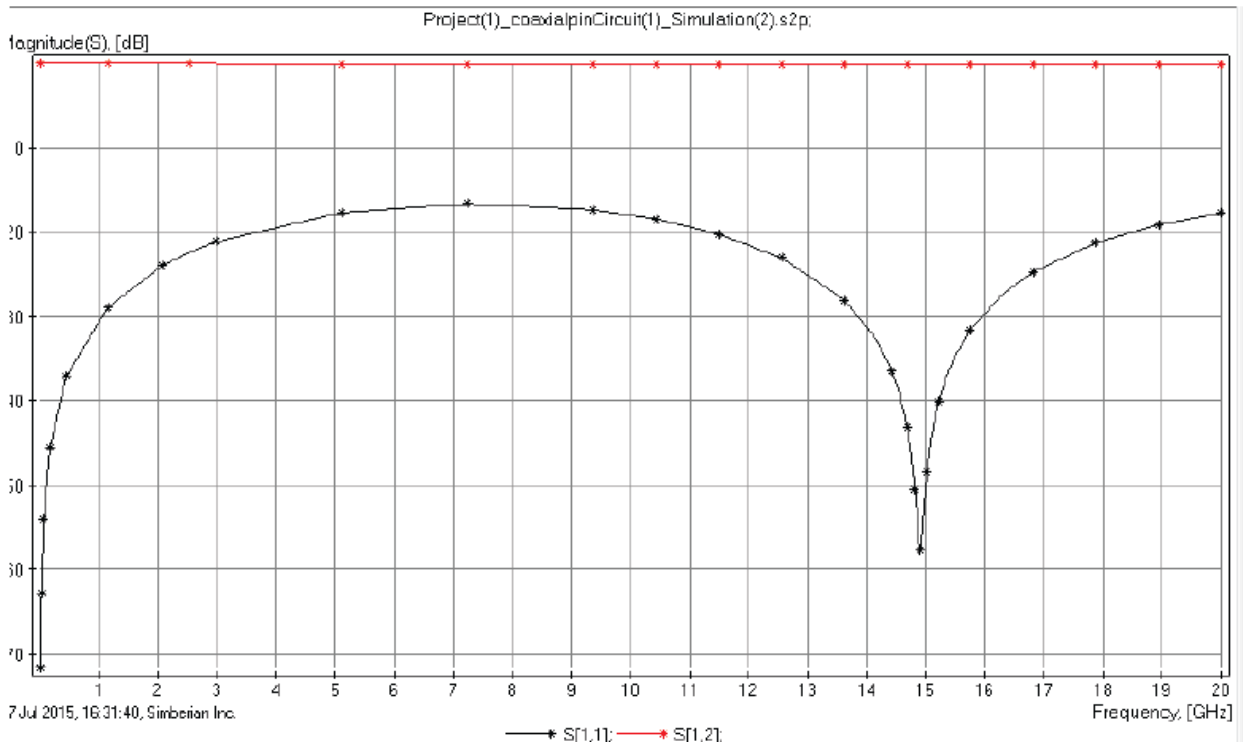


Figure 17
Coaxial Probe S Parameter Modeled

This structure shows less than -0.2dB loss to 20 GHz and much improved return loss as expected. Modeling the coaxial structure including mutual capacitance effects with the channel gives the graph in figure 18

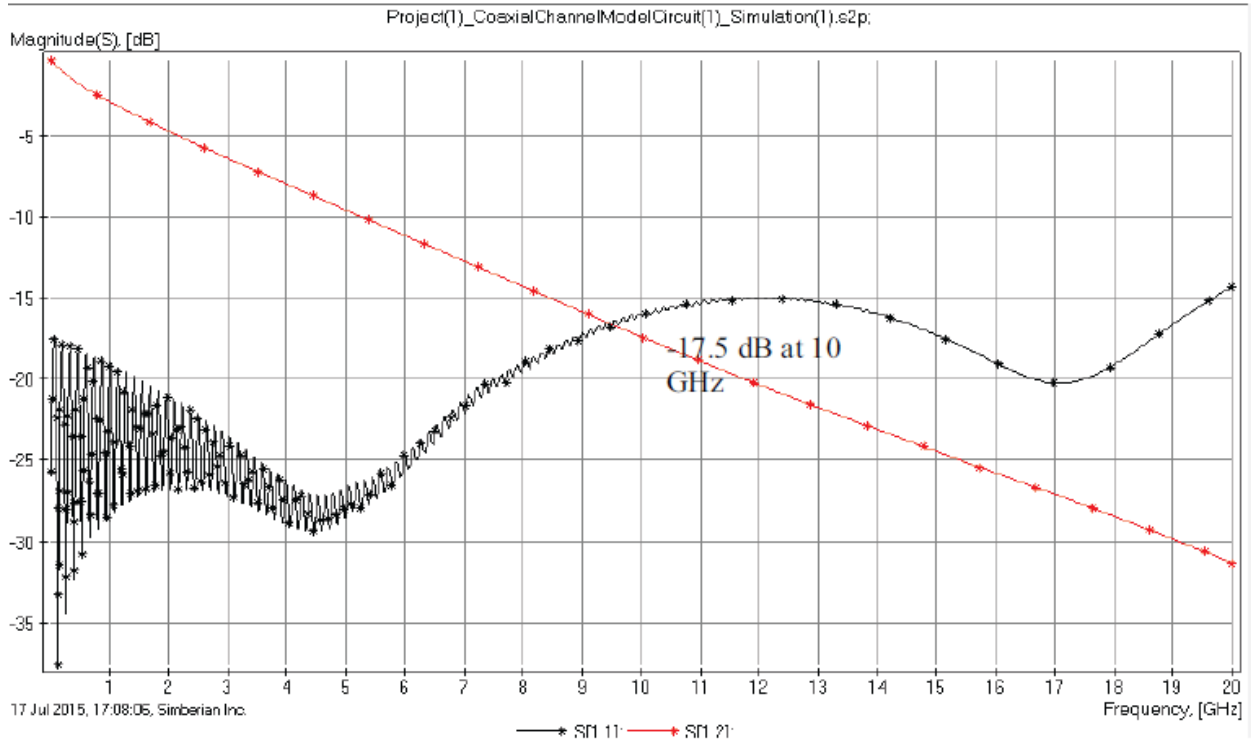


Figure 18
Coaxial Probe Channel Loss

There is a -0.5dB additional loss from the coaxial probe socket or 17.6dB at 10 GHz. Since we achieve the compliance we need with this pin, we have found a solution to long pins with large travel and achieved higher frequency linear performance through 20 GHz.

Comparing all three probes in figure 19:

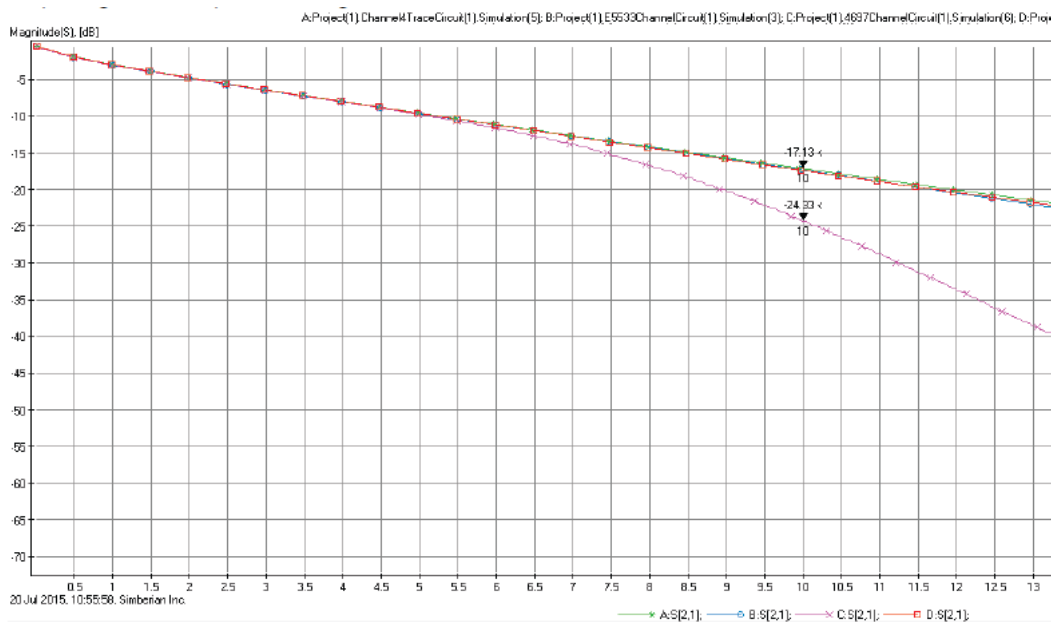


Figure 19 Comparing All Three Probes

The Green trace is the baseline channel, red trace is coaxial pin and blue trace is the E5533 channel. The Magenta channel is the 4697 version with its additional measurably worse high frequency losses.

Conclusion

Converting to a coaxial probe for this application is the solution to achieve test yield above 14 GHz that would be lost with the 4697 probe. The coaxial probe is more complex a solution over the equivalent E5533 but provides the critical compliance needed in this application. In less demanding compliance applications, the E5533 would be the simpler higher frequency choice.

At bit rates above 24GB/s, the cross talk to Insertion loss for this channel intersects so a coaxial structure will most likely provide the best workable solution at bit rates above 20 GB/s a for highly integrated SERDES IO packages. At this level a second study on cross talk and yield should provide documented advantage to the coaxial design in those demanding IO applications requiring pin shielding to improve PLL noise floor, Low voltage noise floors and IO - IO cross talk starting at -24dB.

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