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Case Study
Designing a socket for a 768 Pin BGA Device with 100 W Power and 23 GHz operating Frequency

Notes using SII-B2514-V4 Probe

Design Choices for BGA Socket using Signal Integrity B2514-V4 Probe

- 768 pin BGA Array
- Handler Socket - Package Edge Aligned
- Pin Selection
  - B2514-V4
- Material Selection
  - Vespel SP1   - dK 3.6
- Operating Temperature = 260º C
- Device Current Requirement
  - 2.0 Amps Nominal Continuous Current
- Pin Force 23gr for a total of 16.9 kg to meet 18kg total socket force spec for package

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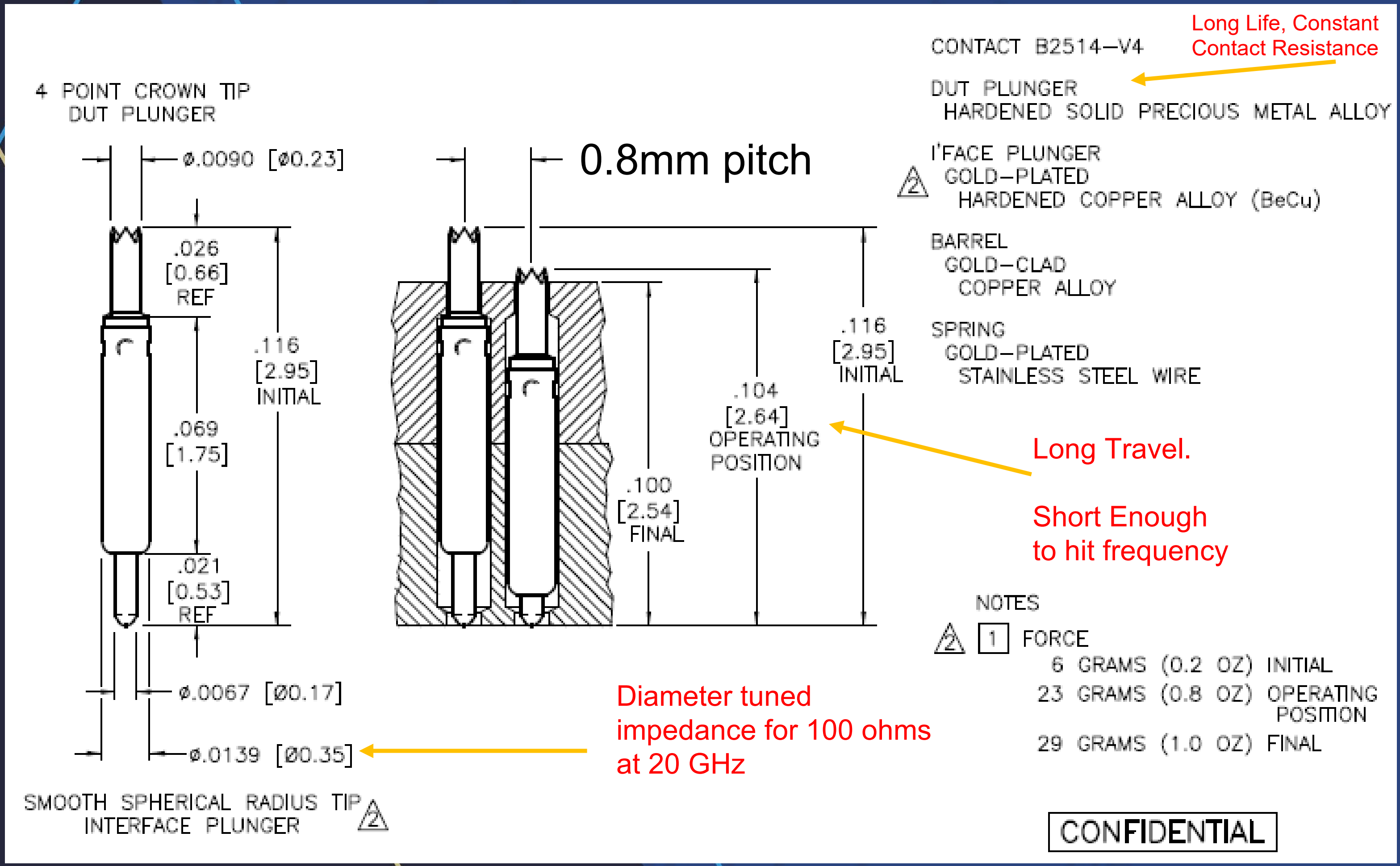
B2514-V4 Probe Pin Design Details



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SII B2514-V4 Pin Design Highlights

- The spring pins are designed with Solid Precious metal Alloy DUT Tip. These un-plated tips provide very long life and can be cleaned with aggressive processes without damaging plating
- The Precious metal plungers are harder than heat treated BeCu. Palladium Alloy- heat treated to 440-470 Hv. Heat treated BeCu is typically 380-420Hv.
- Special alloy Stainless steel springs capable of -60º C to +200º C.
- Signal Integrity Inc. precious metal clad barrels. Clad barrels have 50% thicker precious metal on the bearing surface vs plated barrels.
- Clad material is harder, denser/less porous and more consistent than plated barrels.
- SII Clad process allows us to Clad with different materials on the OD (outer diameter) vs ID (Inner Diameter).
  - OD is clad with a highly conductive Gold Alloy for improved skin effect conductivity.
  - Is ID clad with a hard wear resistant precious metal alloy for improved life on the sliding contact area of barrel ID and plunger surface.

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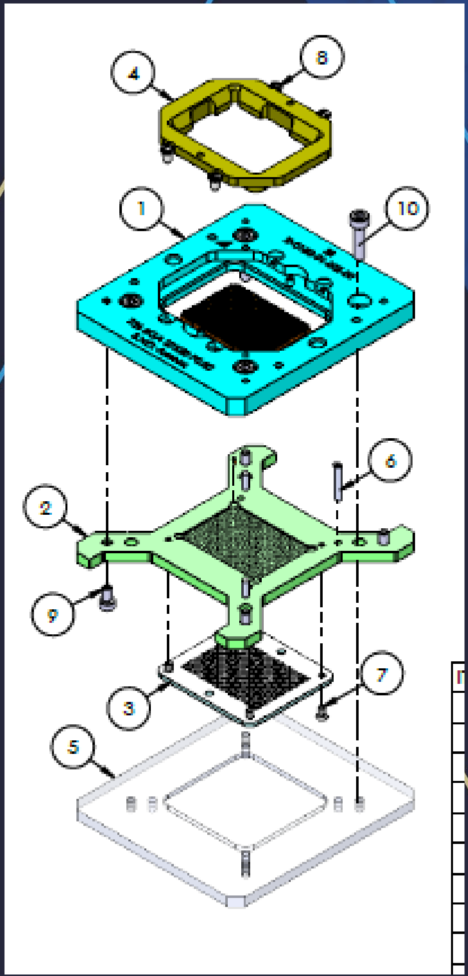
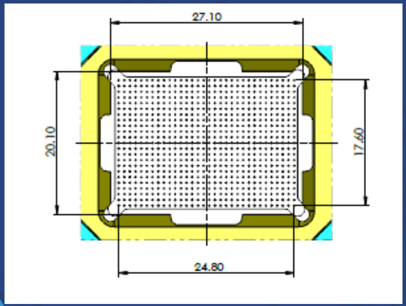
768 pin BGA Socket Design Highlights

Pick and Place Handler Application
Uses an Edge Aligned Nest



#4 – Torlon 5030 Edge Alignment Plate- Designed for Long life under edge flashing wear during part transit



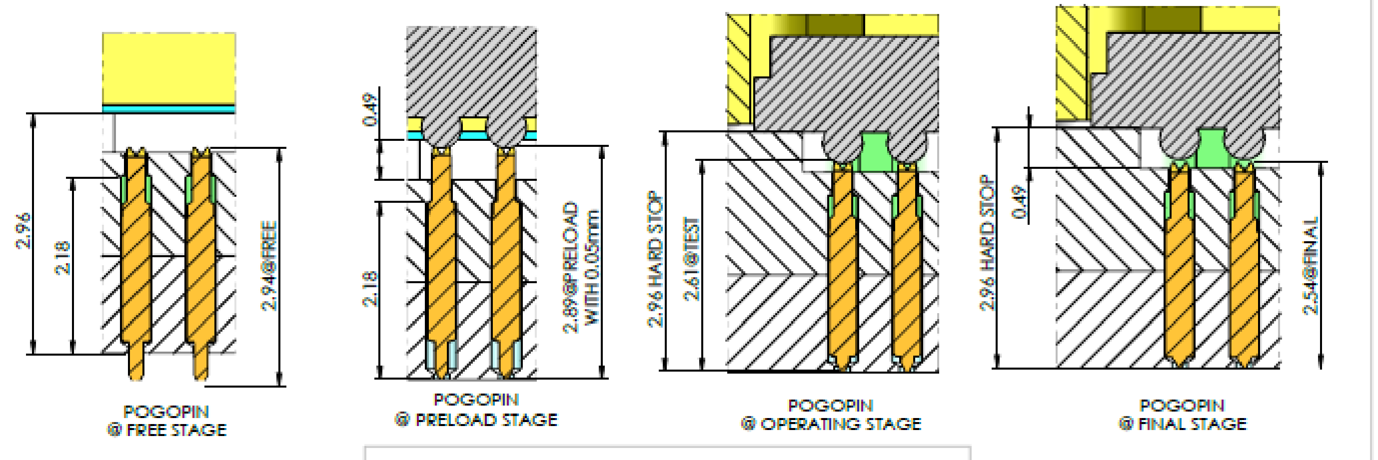
Item #4. Design can be adjusted for package tolerances but is set at nominal at this stage

#1 –Anodized Aluminum Frame. Designed for strength and use in Stainless Steel handler kits.

#2,3 – VESPEL top and bottom pin plate- Designed for strength, drill cavity accuracy and uses a lower dielectric, low glass, high resign material good for high-speed signals. High temperature (260º C).

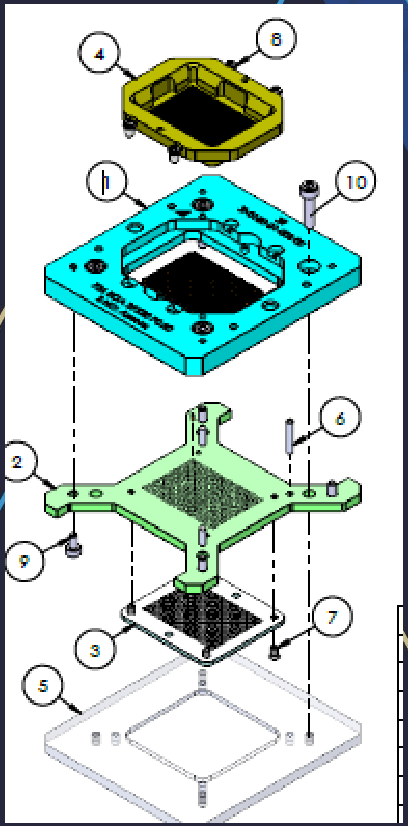
Socket Pin Mechanical Simulation

Edge Alignment



Package Contact Stages for Probe Compression

768 Pad BGA Socket Design Highlights
Floating Nest



- Item #4 is converted to a drilled nest where the BGA balls sit in the nest cavity and align to the pins.

- More complex but is intended to preserve the BGA balls and align more accurately with package variance.

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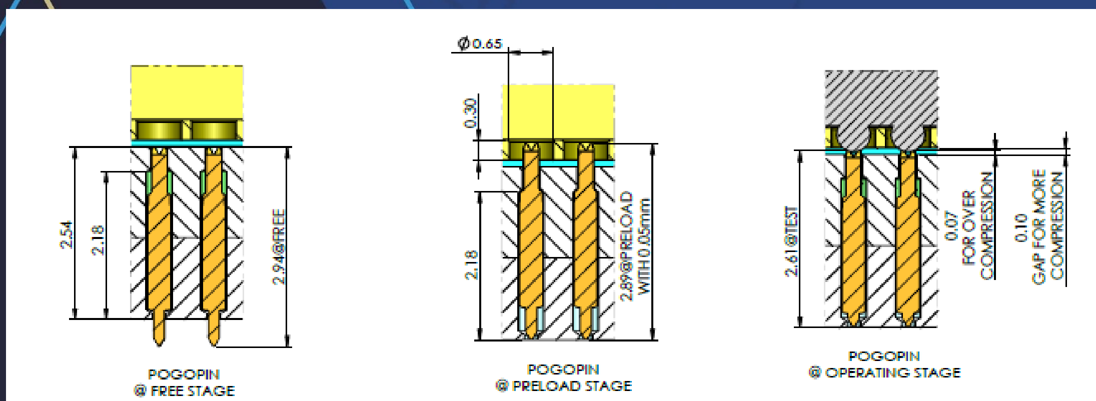
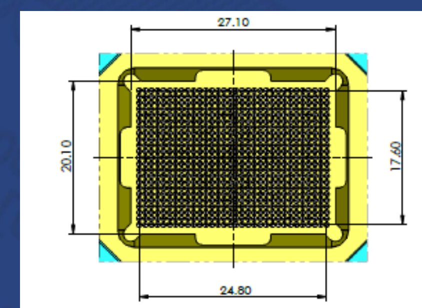
Socket Pin Mechanical Simulation

Nest Alignment



Package Contact Stages for Probe Compression

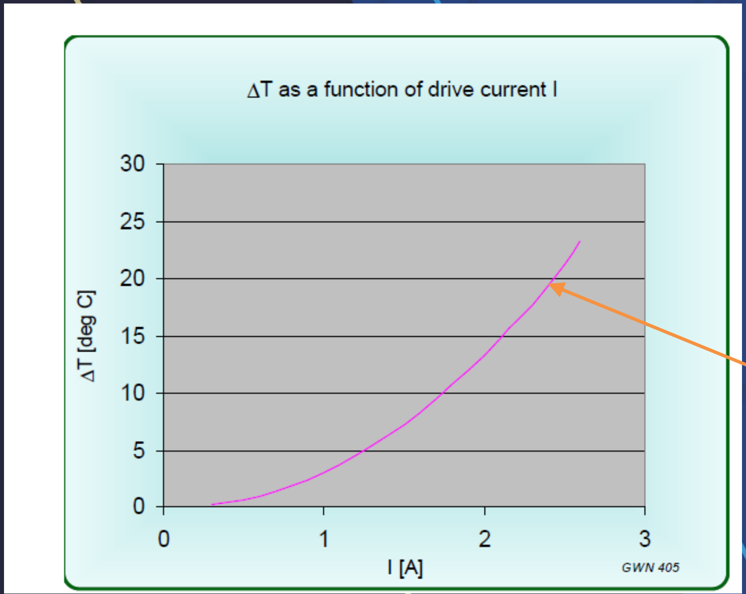
Accurate positioning since it does not need the package outside dimensions to be accurate



Nest design can stress manufacturing since it is more complex.
The thin floor of the drilled nest can be a reliability issue if it cracks under handler Plunger Z-height misalignment.

Confirm that Power And Frequency Performance will Meet Specification to Determine the Probe Selection is Correct

Power Estimate – 100W Total Continuous Power Dissipation



230 power Pins on this Device Package: ½ of these pins supply Vdd at 3.3V maximum

If all Vdd pins are drawing current equally, power per pin is simply 0.75/3.3 or 230mA per power pin pair (Vdd and GND)

The B2514 at 2.4A continuous current can handle 10x this current or the case where 10% of the power pins are carrying all the current. It is sufficient.

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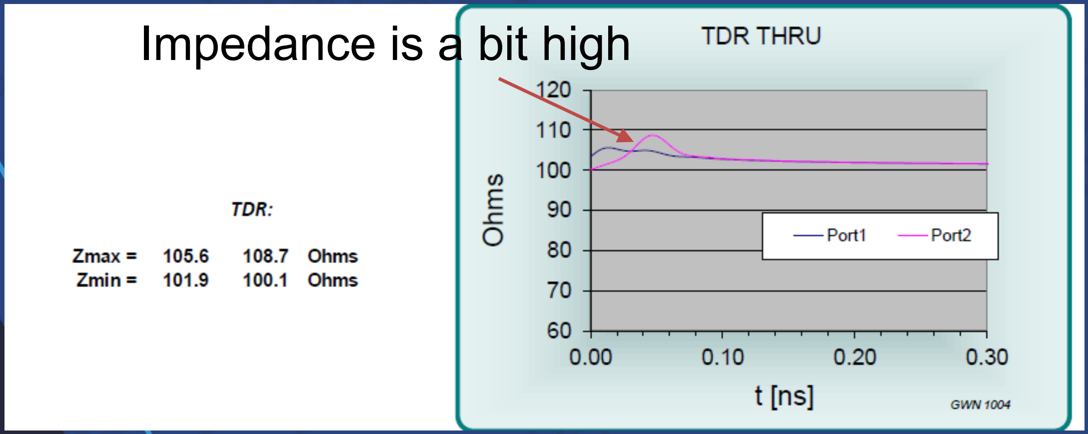
Confirm that Power And Frequency Performance will Meet Specification to Determine the Probe Selection is Correct

Frequency Specification-
PCIGen5 NRZ – 30dB Channel loss Operating Frequency is 23 GHz.

Socket Insertion Loss budget at 23 GHz is -1dB

Impedance target 85 ohms

Impedance Budget 92 Ω ±10% in Test Channel PCB



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Socket Design Summary

- Socket Test Specifications were met or exceeded.
- The cost sensitive nature of this HVM application allowed for more leeway in impedance.
- Impedance mis-match to the test channel had no impact on test performance- yield matched engineering test bed.

This socket design was implemented in High Volume Manufacturing. The impact of an impedance mis-match is difficult to predict from simulation to real test cells. As a rule, impedance should be viewed with insertion loss for broadband signals.

Insertion loss of this socket is out to 24 GHz at -20dB

Impact on the eye closure is minimal